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CLAIMS

1. (Currently amended) An apparatus for converting a non-return-to-zero (NRZ) data signal to a return-to-zero (RZ) data signal, the apparatus comprising an amplifier configured to generate an amplified RZ data signal corresponding to the NRZ data signal based on (i) the NRZ data signal and (ii) a clock signal synchronized with the NRZ data signal, wherein:

the amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal, wherein the differential amplifier comprises a constant current source and two switches connected to the current source, wherein the first and second signals are applied to said two switches to generate the amplified RZ data signal; and there is a DC offset between the first and second signals.

2. (Canceled)

3. (Previously presented) The apparatus of claim 1, wherein the first signal is the NRZ data signal.

4. (Previously presented) The apparatus of claim 1, wherein the width of pulses representing data in the amplified RZ data signal is controlled by the DC offset value.

5. (Previously presented) The apparatus of claim 1, further comprising circuitry configured to condition at least one of the NRZ data signal and the clock signal to produce at least one of the first and second signals.

6. (Previously presented) The apparatus of claim 1, wherein:

(i) if the first signal is greater than the second signal, the amplified RZ data signal is at a low level; and

(ii) if the first signal is less than the second signal, the amplified RZ data signal is at a high level.

7. (Canceled)

8. (Previously presented) The apparatus of claim 1, wherein the amplifier comprises two or more cascaded instances of an amplification stage.

9. (Previously presented) The apparatus of claim 1, wherein the apparatus is implemented as an integrated circuit.

10. (Previously presented) The apparatus of claim 1, wherein:
the NRZ data signal is a trunk NRZ data signal; and

the apparatus further comprises a multiplexer configured to combine two or more tributary NRZ data signals into the trunk NRZ data signal.

11. (Previously presented) The apparatus of claim 10, wherein the multiplexer is further configured to generate the clock signal.